REMARKS

In view of the above amendments and the following remarks, reconsideration and further examination are requested.

First, please note that this amendment is filed concurrently with a Request for Continued Examination. In addition to the present amendment, it is requested in the RCE request that the Amendment filed July 31, 2008 be entered and that the Examiner reconsider the remarks of July 31, 2008 in view of the amendments and remarks herein which address the concerns raised by the Examiner in the Advisory Action of August 13, 2008.

Claims 9-11, 16-19, and 24-27 are pending.

Claims 9-11, 16-19, and 24-27 have been rejected under 35 U.S.C. 103 (a) as being unpatentable over Lasserre (US 6,760,829) in view of Sartorious (US 5,848,436). This rejection is traversed for the following reasons.

In the Advisory Action, the Examiner asserts that "There does not appear to be a limiting definition of the phrase "data structure." The independent claims 9, 16, and 19 as amended herein recite that in the second structure data "data that is smaller than the basic word length is defined to be in an order that is reverse of the defined order in the first structure data."

In the second paragraph of the Advisory Action, the Examiner asserts that "if processors of different endianness were not accessing the same data objects smaller than 32 bits, there would be no need to generate the offsets needed..." However, as in the description in column 9, lines 25-33 of Lasserre, which reads "...offset from the most significant end of the bus if the mode is big endian and from the least significant end if the mode is little endian," Lasserre merely describes that in a big endian processor, [7:0] (data AA) corresponds to byte lane 3, and in a little endian processor, [7:0] corresponds to byte lane 0.

More specifically, since the data input/output terminal D[7:0] of the big endian processor is connected to the most significant address 3 of the memory via a data bus, it can be said that the memory is a big endian memory. Furthermore, since the data input/output terminal D[7:0] of the little endian processor is connected to the least significant address 0 of the memory via the data bus, it can be said that the memory is a little endian memory. This shows that the memory in Fig. 4

represents a big endian memory when accessed by the big endian processor, and represents a little endian memory when accessed by the little endian processor. In other words, the memory during accessing from the big endian processor, and the memory during accessing from the little endian processor are different memories, and Fig. 4 shows the accessing of identical locations in the difference memories.

In the third paragraph of the Advisory Action, the Examiner asserts that "the example does not take into consideration the condition byte complementation performed by address adjustment circuitry 706..." However, as described above, Fig. 4 of Lasserre represents the access to a big endian memory when the access is from the big endian processor, and represents the access to a little endian memory when the access is from a little endian processor, and thus Lasserre fails to disclose applying the address adjustment circuitry 706 in Fig. 7 to Fig. 4. This is clear from the descriptions, "another embodiment" in column 10, lines 42-44, and "if processor core is naturally a little endian processor, then for each transaction access request to a region of memory whose attribute is little endian the physical address is not adjusted" in column 10, line 63 to column 11, line 4.

In view of the above and the remarks in the amendment filed July 31, 2008, entry of which is requested herein, it is submitted that claims 9-11, 16-19, and 24-27 are allowable over the prior art of record and that the present application is in condition for allowance. The Examiner is invited to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,

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